A Low Phase Noise C-Band Frequency Synthesizer Using a New Fractional-N PLL with Programmable Fractionality

Tadao Nakagawa and Tsuneo Tsukahara

Abstract— **This paper presents a new fractional-N PLL that has an arbitrary denominator of the fractional division ratio as well as an arbitrary numerator and an integer part. This enables a reduction in the phase noise of frequency synthesizers for many applications with various channel-space frequencies. The circuit elements of this fractional-N PLL are fabricated in LSI's that operate up to 6.5 GHz. They have been successfully installed in a C-band frequency synthesizer with a low phase noise MMIC VCO.**

I. Introduction

The frequency synthesizer is a key device in radio systems. Most microwave frequency synthesizers use phase-locked loops (PLL's) to improve frequency stability. For many synthesizer applications, fine resolution is important. As the frequency step size decreases, however, the division ratio between an output microwave frequency and the reference frequency increases; the higher the division ratio is, the worse the phase noise within the loop bandwidth becomes. Low phase noise is particularly important in communication systems using phase modulation, which are becoming more and more common nowadays. Although synthesizers comprising more than one PLL have ordinarily been used to meet both phase noise and step size requirements, a single-loop scheme is attractive for its simplicity.

Phase noise in single loops can be reduced by making the reference frequency higher than the step size through the use of the fractional-N configuration [1]–[4] or pulse insertion [5], [6]. Unfortunately, the fractionality of conventional fractional-N PLL's is fixed; thus they lack flexibility: new applications require new hardware design. The pulse insertion technique provides more flexibility, but an additional delay line is required.

This paper presents a new fractional-N PLL that features an arbitrary denominator of the fractional division ratio and, hence, application versatility. Circuit elements are fabricated in LSI's that operate up to 6.5 GHz. Combining these LSI's with an MMIC VCO having a planar resonator results in a very low phase noise C-band frequency synthesizer.

II. Conventional Fractional-N PLL

Fig. 1 is a block diagram of a conventional fractional-N PLL [1–4]. The accumulator consists of an n-bit full adder and an n-bit latch. The content of the accumulator increases by control word K each reference frequency cycle. When the accumulator content amounts to or exceeds 2^n, it generates an overflow signal. This signal is fed to a programmable counter to alter the integer division ratio of the divider N to $N+1$ periodically. Note that when the input frequency is high the programmable counter is replaced with a pulse-swallow counter, which consists of a dual-modulus prescaler and two programmable counters. The resulting average division ratio N_{AVE} is given by

$$N_{\mathrm{AVE}} = \frac{K \cdot (N+1) + (2^n - K) \cdot N}{2^n} = N + \frac{K}{2^n} \tag{1}$$

Thus, the voltage-controlled oscillator (VCO) frequency f_{VCO} is

$$f_{\mathrm{VCO}} = N_{\mathrm{AVE}} \cdot f_{\mathrm{REF}} = \left(N + \frac{K}{2^n}\right) \cdot f_{\mathrm{REF}} \tag{2}$$

where f_{REF} is the reference frequency. The step size obtained by changing K to $K+1$ is equal to $f_{\mathrm{REF}}/2^n$, i.e., the reference frequency can be made 2^n times higher than a given step size, thereby suppressing phase noise. However, current fractional-N PLL's have a drawback: the n of 2^n is fixed because it is the bit number determined by the hardware. The relationship between the reference frequency that adequately suppresses phase noise and the given step size varies for different application, which means new applications need new designs.

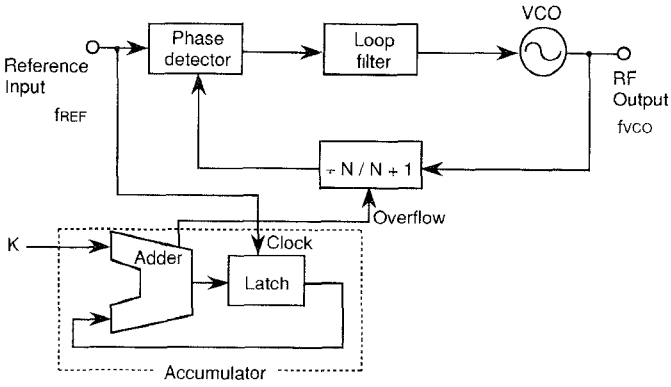

Fig. 1. Block diagram of conventional fractional-N PLL's.

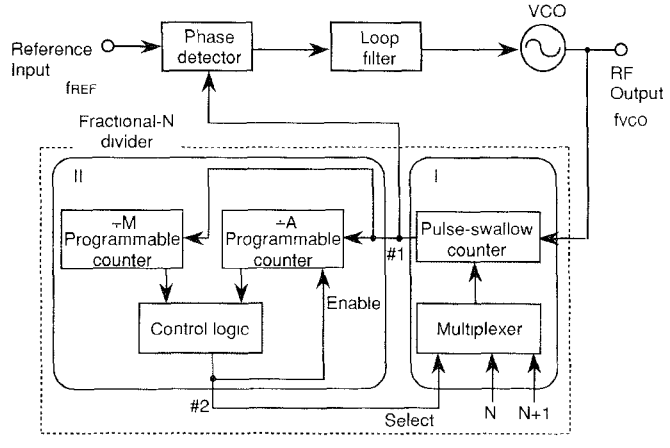

Fig. 2. New fractional-N PLL.

III. New Fractional-N PLL

A. Structure and Operation

A block diagram of the new fractional-N PLL is shown in Fig. 2, and its timing chart is shown in Fig. 3. The fractional-N divider part

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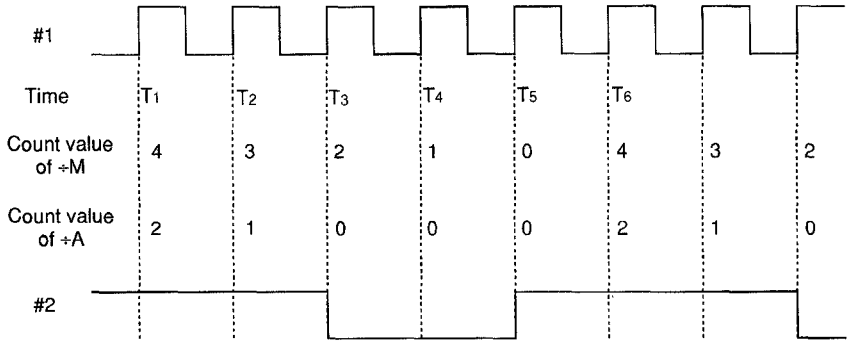

Fig. 3. Timing chart of the new fractional-N PLL.

consists of a programmable counter ($\div M$), another programmable counter with an enable input ($\div A$), a control logic unit, a multiplexer whose output is selected from two input data by a select terminal input, and an ordinary pulse-swallow counter. When the $\div M$ counter is programmed to $M-1$, and the $\div A$ counter is programmed to $A-1$ ($A \leq M$), the count values decrease one by one at every output of the pulse-swallow counter (#1 in the figures). The control logic output (#2) is low when $A=0$ and $M \neq 0$. The output is high in other cases. The timing chart shown in Fig. 3 is the case when $M=5$ and $A=3$. At T_3, the count value of the $\div A$ counter becomes 0 and the control logic output (#2) changes from high to low. Since the output is connected to the enable terminal of the $\div A$ counter, this counter stops the counting operation. At T_5, the control logic output again becomes high, and the two counters are again set to the initial values, $M-1$ and $A-1$, at the next clock edge, T_6. As a result, the control logic output is high when the pulse-swallow counter generates A pulses and low when the pulse-swallow counter generates $(M-A)$ pulses. This output is also fed to the select terminal of the multiplexer that is given the two data N and $N+1$. This multiplexer provides the pulse-swallow counter with a division ratio setting. If the multiplexer output is $N+1$ at the high state of the select signal and N at the low state, the resulting average division ratio of the pulse-swallow counter N_{AVE} is

$$N_{\mathrm{AVE}} = \frac{A \cdot (N+1) + (M-A) \cdot N}{M} = N + \frac{A}{M}. \tag{3}$$

This equation shows the division ratio consists of an integral part, N, and a fractional part, A/M. In the PLL, the VCO frequency f_{VCO} is

$$f_{\mathrm{VCO}} = N_{\mathrm{AVE}} \cdot f_{\mathrm{REF}} = \left(N + \frac{A}{M}\right) \cdot f_{\mathrm{REF}}. \tag{4}$$

The N, A, and M in this equation are all programmable. The new PLL therefore has large flexibility for various applications. Because of the simple control circuitry among the programmable counters, including the pulse-swallow counter, the divider operates at high speed. The configuration of the new fractional-N divider is, so to speak, a dual-loop pulse-swallow counter scheme.

B. LSI Fabrication

The fractional-N divider was fabricated on two LSI's by Si super self-aligned process technology [7]. The pulse-swallow counter and the multiplexer are integrated on a 5.0×4.0 mm chip (Chip I); and the two programmable counters and the control logic are integrated on a 6.5×6.5 mm chip (Chip II). The latter chip is larger because its fabrication process is gate array while the former uses a custom process. The integrated pulse-swallow counter consists of a $\div 4/\div 5$ dual-modulus prescaler, a 10-bit programmable counter and a 2-bit swallow counter. The multiplexer section consists of a dozen two-channel multiplexers that incorporate a common data select input. Both the $\div M$ counter and $\div A$ counter are 8-bit programmable counters.

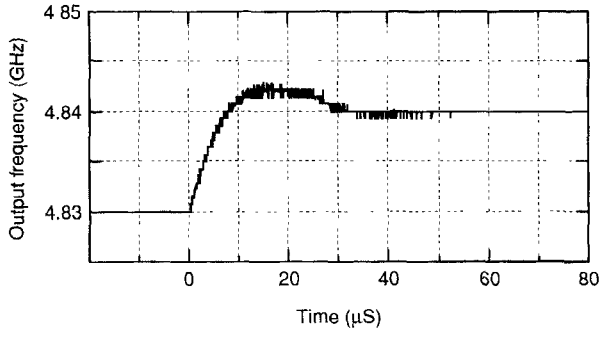

Fig. 4. Frequency transition response.

IV. Experimental Results

The measured input minimum power of Chip I is -20 dBm at 2 GHz, -15 dBm at 4 GHz, and $+5$ dBm at 6.5 GHz. The LSI operates up to 6.5 GHz. This upper-limit frequency is mainly determined by the performance of the dual-modulus prescaler in the pulse-swallow counter.

The new fractional-N PLL shown in Fig. 2 was achieved in hardware in conjunction with a C-band MMIC VCO having a planar resonator [8]. A Si bipolar transistor is used as the active device of the VCO because of its low $1/f$ noise. The planar resonator is actually a microstrip line resonator with a gold conductor and alumina substrate. The VCO's tuning range is between 4.7 and 4.9 GHz. As the phase detector in Fig. 2, a phase frequency comparator (PFC) was employed here.

When the denominator of the fractional division ratio $M=8$ and the reference frequency is 80 MHz, phase locking is achieved. Fig. 4 shows the frequency transition response measured when the division ratio is changed from $60+3/8$ to $60+4/8$. A 10-MHz frequency step is successfully obtained after about 50-μs pull-in time, even though the reference frequency is 80 MHz. The spurs at 10-MHz offset is -57 dBc. This spur level is tolerable for many applications, but it is higher than the level for the frequency synthesizer using pulse

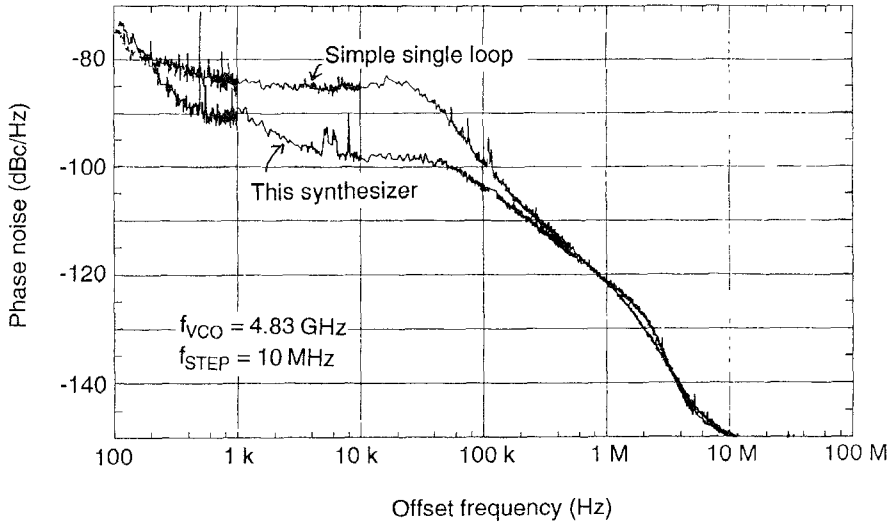

Fig. 5. Phase noise performance

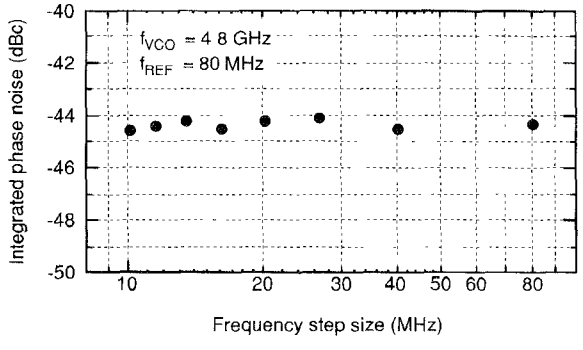

Fig. 6. Phase noise vs different step sizes.

insertion of −65 dBc [5, 6] because fractional-N PLL's, including this one, modify their division ratio periodically.

The phase noise performance is shown in Fig. 5, where it is compared with a simple single-loop synthesizer with the same step size whose division ratio is an integer. The phase noise of the new synthesizer is about 15 dB lower.

Figure 6 shows the integrated single sideband phase noise against the frequency step size of the new synthesizer. The integral region is from 100 Hz to 10 MHz from the carrier. In this measurement, the reference frequency was fixed at 80 MHz, and then the denominator of the fractional division ratio M was changed. This change could be easily made by only programming. The phase noise performance is steady for the different step sizes.

V. Conclusion

A new fractional-N PLL has been developed that features a programmable fractional division ratio. The circuit elements of this fractional-N PLL were fabricated in LSI's that operate up to 6.5 GHz. Combining them with an MMIC VCO having a planar resonator results in a very low phase noise C-band frequency synthesizer. This technique provides large flexibility and can be applied to most microwave synthesizers.

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